Asynchronous Circuit Verification Using Trace Theory and CCS

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Abstract

We investigate asynchronous circuit verification using Dill's trace theory [1] as well as Milner's CCS (as mechanized by the Concurrency Workbench). Trace theory is a formalism specifically designed for asynchronous circuit specification and verification. CCS is a general purpose calculus of communicating systems that is being recently applied for hardware specification and verification [2]. Although both formalisms are similar in many respects, we find that there are many interesting differences between them when applied to asynchronous circuit specification and verification. The purpose of this paper is to point out these differences, many of which are precautions for avoiding writing incorrect specifications. A long-term objective of this work is to find a way to take advantage of the strengths of both the Trace Theory verifier and the Concurrency Workbench in verifying asynchronous circuits.