Automatic Rapid Prototyping of Semi-Custom VLSI Circuits using FPGAs

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Abstract

We describe a technique for translating semi-custom VLSI circuits automatically, integrating two design environments, into field programmable gate arrays (FPGAs) for rapid and inexpensive prototyping. The VLSI circuits are designed using a cell-matrix based environment that produces chips with density comparable to full custom VLSI design. These circuits are translated automatically into FPGAs for testing and system development. A four-bit pipelined array multiplier is used as an example of this translation. The multiplier is implemented in CMOS in both synchronous and asynchronous pipelined versions, and translated into Actel FPGAs both automatically, and by hand for comparison. The six test chips were all found to be fully functional, and the translation efficiency in terms of chip speed and area is shown. This result demonstrates the potential of this approach to system development.