

# Timing Constraints for High Speed Counterflow-Clocked Pipelining

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UUCS-95-019

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October 30, 1995

## Abstract

*With the escalation of clock frequencies and the increasing ratio of wire- to gate-delays, clock skew is a major problem to be overcome in tomorrow's high-speed VLSI chips. Also, with an increasing number of stages switching simultaneously comes the problem of higher peak power consumption. In our past work, we have proposed a novel scheme called Counterflow-Clocked( $C^2$ ) Pipelining to combat these problems, and discussed methods for composing  $C^2$  pipelined stages. In this paper, we analyze, in great detail, the timing constraints to be obeyed in designing basic  $C^2$  pipelined stages as well as in composing  $C^2$  pipelined stages.  $C^2$  pipelining is well suited for systems that exhibit mostly uni-directional data flows as well as possess mostly nearest-neighbor connections. We illustrate  $C^2$  pipelining on such a design with several design examples.  $C^2$  pipelining eases the distribution of high speed clocks, shortens the clock period by eliminating global clock signals, allows natural use of level-sensitive dynamic latches, and generates less internal switching noise due to the uniformly distributed latch operation. By applying  $C^2$  pipelining and its composition methods to build a system, VLSI designers can substitute the global clock skew problem with many local one-sided delay constraints.*