Architectural Considerations in a Self-Timed Processor Design

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Abstract

There are fundamental differences in the structure of asynchronous and synchronous processors, and the problems of each approach require innovative solutions. This work explores some of the ways in which the structure of a specific design is affected by an asynchronous paradigm. The Fred architecture presented here is an example of such a design approach. The self-timed design philosophy directly results in a powerful and flexible architecture which exhibits significant savings in design effort and circuit complexity. Some of the architectural constraints discovered in the course of the research have simple yet unconventional solutions, which in turn provide additional benefits beyond their immediate application. Further, when an asynchronous philosophy is incorporated at every stage of the design, the microarchitecture is more closely linked to the basic structures of the self-timed circuits themselves, and the resulting processor is quite surprising in its simplicity and elegance.