A DRAM Backend for The Impulse Memory System

Lixin Zhang

UUCS-00-002

Department of Computer Science
University of Utah
Salt Lake City, UT 84112, USA

December 16, 1998

Abstract

The Impulse Adaptable Memory System exposes DRAM access patterns not seen in conventional memory systems. For instance, it can generate 32 DRAM accesses each of which requests a four-byte word in 32 cycles. Conventional DRAM backends are optimized for accesses that request full cache lines. They may not be able to handle smaller accesses effectively.

In this document, we describe and evaluate a DRAM backend that reduces the average DRAM access latency by exploiting the potential parallelism of DRAM accesses in the Impulse system. We design the DRAM backend by studying each of its important design options: DRAM organization, hot row policy, dynamic reordering of DRAM accesses, and interleaving of DRAM banks. The experimental results obtained from the execution-driven simulator Paint [10] show that, compared to a conventional DRAM backend, the proposed backend can reduce the average DRAM access latency by up to 98%, the average memory cycles by up to 90%, and the execution time by up to 80%.

This effort was sponsored in part by the Defense Advanced Research Projects Agency (DARPA) and the Air Force Research Laboratory (AFRL) under agreement number F30602-98-1-0101 and DARPA Order Numbers F393/00-01 and F376/00. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official polices or endorsements, either express or implied, of DARPA, AFRL, or the US Government.