Formal Specification of the Virtual Component Interface Standard in the Unified Modeling Language

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Abstract

As part of our charge from the Virtual Sockets Interface Alliance we search for a notation in which standards documents can be precisely specified. We approach the specification for standard problem in the context of the Virtual Component Interface Standard. We propose six orthogonal axes of specification as guides to creating a cohesive, well-rounded requirements specification. We then specify the Virtual Component Interface Standard in the Unified Modeling Language and evaluate that specification based on our six axes.

1   Introduction

The recent excitement over system-on-chip (SoC) systems raises the bar for formal methods techniques and tools. Not only do we face the usual challenges of keeping development costs low, keeping time-to-market small and ensuring high quality hardware, but now, we also face the challenge of integrating externally developed hardware and accompanying proofs into our overall design and verification strategy.