Analyzing the Intel Itanium Memory Ordering Rules Using Logic Programming and SAT

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Abstract

We present a non-operational approach to specifying and analyzing shared memory consistency models. The method uses higher order logic to capture a complete set of ordering constraints on execution traces, in an axiomatic style. A direct translation of the semantics to a constraint logic programming language provides an interactive and incremental framework for exercising and verifying £nite test programs. The framework has also been adapted to generate equivalent boolean satis£ability (SAT) problems. These techniques make a memory model speci£cation executable, a powerful feature lacked in most non-operational methods. As an example, we provide a concise formalization of the Intel Itanium memory model and show how constraint solving and SAT solving can be effectively applied for computer aided analysis. Encouraging initial results demonstrate the scalability for complex industrial designs.