Automating the Design of Embedded Domain Specific Accelerators

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UUCS-08-002

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February 20, 2008

Abstract

Domain specific architecture (DSA) design currently involves a lengthy process that requires significant designer knowledge, experience, and time in arriving at a suitable code generator and architecture for the target application suite. Given the stringent time to market constraints and the dynamic nature of embedded applications, designers face a huge challenge in delivering high performance yet energy efficient devices. In this study, we investigate an automatic design space exploration tool that employs an iterative technique known as "Stall Cycle analysis" (SCA) to arrive at near-optimal energy-performance designs for various constraints ,e.g., minimum area. For each design candidate in the process, the results of code generation and simulation are analyzed to identify bottlenecks to performance (or energy) and provide insight into adding or removing resources for further improvements. Second, we demonstrate the utility of exploration in pruning the design space effectively (from $\geq$1000 points to tens of points) for three application domains: face recognition, speech recognition, and wireless telephony. As compared to manual designs optimized for a particular metric, SCA automates the design of DSAs for minimum energy-delay product (17% improvement for wireless telephony), minimum area (75% smaller design for face recognition), or maximum performance (38% improvement for speech recognition). Finally, we discuss the impact of per design code generation in reducing DSA design time from man-months to hours and in identifying superior design points through architectural design space exploration.