250P Computer Systems Architecture, Winter 2019

DFS
DVFS

Adapted from Rajeev Subramanium's Spring '16 CS6810 course (University of Utah)

28 Jan 2019

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Basic idea of DFS and DVFS

We need to improve the performance of the processor:
i.e., reduce its power and energy consumption.

two techniques to so:

Dynamic Frequency Scaling - change frequency of processor
Dynamic Voltage and Frequency Scaling - change V and f of processor during runtime

both impacts the *power consumption* and *time* of the processor

Example of how DFS and DVFS changes power and time of processor

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> Change frequency to 0.5 GHz
> So new cycle time = 2 ns

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Note

> Each circuit has been designed to complete within 1 ns.
> So now, each circuit has enough time to finish the task assigned to it.

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> Decreasing the frequency is ok.
> Increasing the frequency is not an option -- because would then be assigning a new task to a circuit before it could finish.

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What is the,
New Execution Time?
New Energy Consumption?
New Power Consumption?

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Two relations

Dynamic Power α Voltage^2 x Frequency

Leakage Power α Voltage x Leakage Current

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[White-Board]

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> Program is entirely CPU-bound.

> In reality, programs may be memory bound. Memory is not affected by CPU speed.

A memory bound program

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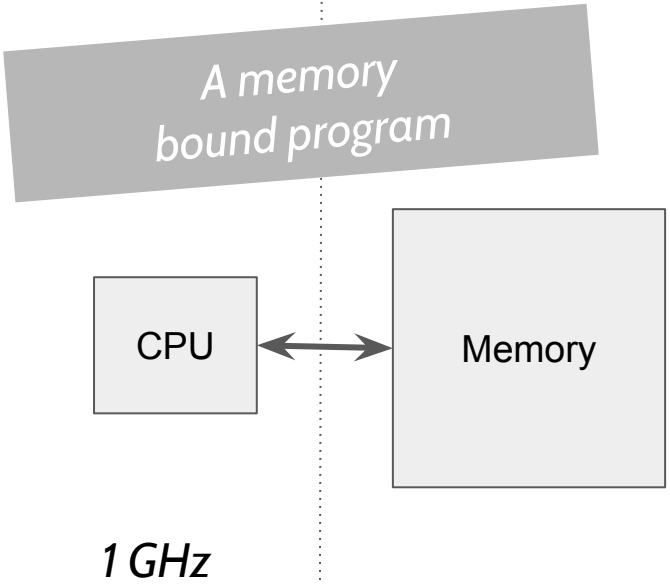

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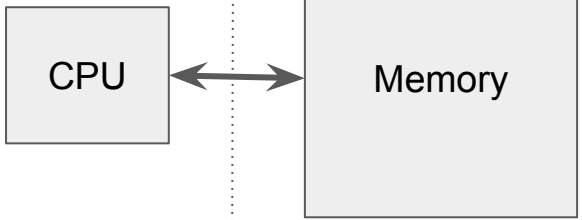

1 GHz

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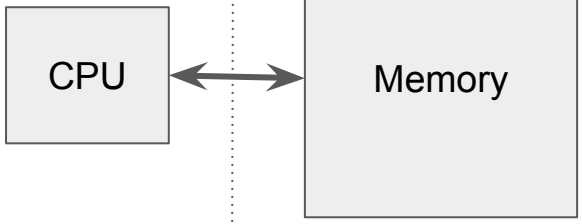

1 GHz — *100 ns for a memory read* = *100 cycles*

0.5 GHz — *100 ns for a memory read* = *50 cycles*

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If this example program was memory-bound the total time taken would have been less than 200s.

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Summarizing DFS,

> Reducing frequency can significantly reduce power.

> Reducing frequency may not necessarily reduce energy due to a (possibly linear) increase in execution time.

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Applying DVFS,

> Change supply voltage to 0.9 V
> Also need to reduce frequency, because circuit delay increases if V decreases.

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[White-Board]

Problem 3 on Rajeev's Slides (Slide nos. 10, 11)

Thank you